WHAT IS CLAIMED IS:

1. A method for controlling a phase locked loop in a computer system clock generator comprising the steps of:

generating a lead error signal when a first signal leads a second signal and a lag error signal when said first signal lags said second signal;

generating a phase error signal in response to said lead error signal and said lag error signal;

generating a variable first gain signal in response to said phase error signal and said first signal;

generating a variable second gain signal in response to said lead error signal and said lag error signal;

generating a control signal in response to a first reference signal, a second reference signal, said first gain signal and said second gain signal; and

applying said control signal to a voltage controlled oscillator as a frequency control signal of an output of a voltage controlled oscillator generating said second signal.

2. The method of claim 1, wherein said lead error signal is a logic one pulse if said first signal leads said second signal during a cycle of said second signal and said lag error signal is a logic one pulse if said first signal lags said second signal during said cycle of said second signal.

3. The method of claim 1, wherein said phase error signal is increased on a transition of said lead error signal and decreased on a transition of said lag error signal.

4. The method of claim 1, wherein said first gain signal is increased if an absolute value of said phase error signal reaches a first threshold value within a time window and decreased if said absolute value of said phase error signal does not reach said first threshold value in said time window.

5. The method of claim 1, wherein said second gain signal is a value $+K$ if said lead error signal is a logic one pulse and a value $-K$ if said lag error signal is a logic one pulse, wherein K is a numerical value including the value one.

6. The method of claim 1, wherein said first gain signal is limited to a magnitude between a predetermined maximum level and a predetermined minimum level.

7. The method of claim 6, wherein a third signal is generated by adding said first reference signal to said second reference signal multiplied by said first gain signal.

8. The method of claim 7, wherein said control voltage is generated in response to said third signal, an integral of said third signal, and said second gain signal.

9. The method of claim 8, wherein said third signal is multiplied by said second gain signal generating a modified third signal.

10. The method of claim 9, wherein said control voltage is generated by adding said modified third signal multiplied by a first constant to an integral of said modified third signal multiplied by a second constant.

11. The method of claim 1, wherein said first threshold value and said time window are dynamically variable.

12. A phase locked loop (PLL) comprising:

a phase comparator receiving a first signal and a second signal and generating a lead error signal when said first signal leads said second signal and a lag error signal when said first signal lags said second signal;

a phase error generator for generating a phase error signal in response to said lead error signal and said lag error signal;

a circuit for generating a variable first gain signal in response to said phase error signal and said first signal;

a circuit for generating a variable second gain signal in response to said lead error signal and lag error signal;

a circuit for generating a control signal in response to a first reference signal, a second reference signal, said first gain signal and said second gain signal; and

a voltage controlled oscillator receiving said control signal as a frequency control signal of an output of said voltage controlled oscillator generating said second signal.

13. The PLL of claim 12, wherein said lead error signal is a logic one pulse if said first signal leads said second signal during a cycle of said second signal and said lag error signal is a logic one pulse if said first signal lags said second signal during said cycle of said second signal.

14. The PLL of claim 12, wherein said phase error signal is increased on a transition of said lead error signal and decreased on a transition of said lag error signal.

15. The PLL of claim 12, wherein said first gain signal is increased if an absolute value of said phase error signal reaches a first threshold value within a time window and

decreased if said absolute value of said phase error signal does not reach said first threshold value in said time window.

16. The PLL of claim 12, wherein said second gain signal is a value $+K$ if said lead error signal is a logic one pulse and a value $-K$ if said lag error signal is a logic one pulse, wherein K is a numerical value including the value one.

17. The PLL of claim 12, wherein said first gain signal is limited to a magnitude between a predetermined maximum level and a predetermined minimum level.

18. The PLL of claim 17, wherein a third signal is generated by adding said first reference signal to said second reference signal multiplied by said first gain signal.

19. The PLL of claim 18, wherein said control voltage is generated in response to said third signal, an integral of said third signal, and said second gain signal.

20. The PLL of claim 19, wherein said third signal is multiplied by said second gain signal generating a modified third signal.

21. The PLL of claim 20, wherein said control voltage is generated by adding said modified third signal multiplied by a first constant to an integral of said modified third signal multiplied by a second constant.

22. The PLL of claim 12, wherein said first threshold value and said time window are dynamically variable.

23. A data processing system comprising:

a processor central processing unit (CPU);

a random access memory (RAM);

a read only memory (ROM); and

a bus system coupling said CPU to said ROM and said RAM, said CPU further comprising a phase locked loop (PLL) in clock generator, said PLL comprising:

circuitry for receiving a first signal and a second signal and generating a lead error signal when said first signal leads said second signal and a lag signal when said first signal lags said second signal;

circuitry for generating a phase error signal in response to said lead error signal and said lag error signal;

circuitry for generating a variable first gain signal in response to said phase error signal;

circuitry for generating a variable second gain signal in response to said lead error signal and lag error signal;

circuitry for generating a control signal in response to a first reference signal, a second reference signal, said first gain signal and said second gain signal; and

a voltage controlled oscillator receiving said control signal as a frequency control signal for an output of said voltage controlled oscillator generating said second signal.

24. The data processing system of claim 23, wherein said lead error signal is a logic one pulse if said first signal leads said second signal during a cycle of said second signal and said lag error signal is a logic one pulse if said first signal lags said second signal during said cycle of said second signal.

25. The data processing system of claim 23, wherein said phase error signal is increased on a transition of said lead error signal and decreased on a transition of said lag error signal.

26. The data processing system of claim 23, wherein said first gain signal is increased if an absolute value of said phase error signal reaches a first threshold value within a time window and decreased if said absolute value of said phase error signal does not reach said first threshold value in said time window.

27. The data processing system of claim 23, wherein said second gain signal is a value $+K$ if said lead error signal is a logic one pulse and a value $-K$ if said lag error signal is a logic one pulse, wherein K is a numerical value including the value one.

28. The data processing system of claim 23, wherein said first gain signal is limited to a magnitude between a predetermined maximum level and a predetermined minimum level.

29. The data processing system of claim 28, wherein a third signal is generated by adding said first reference signal to said second reference signal multiplied by said first gain signal.

30. The data processing system of claim 29, wherein said control voltage is generated in response to said third signal, an integral of said third signal, and said second gain signal.

31. The data processing system of claim 30, wherein said third signal is multiplied by said second gain signal generating a modified third signal.

32. The data processing system of claim 31, wherein said control voltage is generated by adding said modified third signal multiplied by a first constant to an integral of said modified third signal multiplied by a second constant.